IGNITE™ Core Family

Based on the patented ShBoom™ architecture, the IGNITE family of processor cores provides an unparalleled price/performance advantage for a wide range of embedded applications. The unique architecture is a blend of the best stack- and register-based designs with 8-bit instructions for enhanced performance and optimal code size.

The IGNITE architectural philosophy is to provide the simplest solution while best utilizing existing resources. This typically means fewer transistors, translating into lower power consumption. The low gate count results in significantly lower manufacturing costs.

Designed with system OEMs and semiconductor manufacturers in mind, the IGNITE family of cores is perfectly suited for those who want to rapidly integrate their own custom logic and peripherals with a low-cost, low-power, high-performance RISC processor. Due to the ease of integration and portability, manufacturers are able to dedicate more attention to end-user products.

The design is available in VHDL and Verilog formats as a synthesizable net list, and can be procured through flexible licensing arrangements.

FEATURES

- 600MHz operation in 0.13 micron technology
- Optimized 32-bit hybrid RISC/stack processor architecture
- Low transistor count and no cache requirements
- 32-bit wide multi-instruction fetch
- Available in VHDL and Verilog formats
- Simulation in custom FPGA hard-ware environment (SEP)

BENEFITS

- Industry's EEMBC performance-density leader (Consumermark)
- Uniquely suited for real-time applica-tions through efficient stack-based context
- Ideal design for SoCs

APPLICATIONS

- Internet
- Service gateways
- Home and business automation
- Cellular phones
- PDAs
- Wireless devices
- Smart cards
- Transaction processing
- E-commerce
- Consumer and industrial

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Hardware Specifications

- Die size of .43 sq mm
- Performance of 1MIPS per MHz
- Power dissipation of 0.22 milliWatts per MHz
- Idle power less than 46 microWatts
- Power/performance factor of 4545 MIPS per watt
- Worst case and typical operating frequencies of 225 and 360 MHz
- 4 gigabytes of physical address space
- 8-level interrupt controller
- Dedicated 8 inputs and 8 outputs
- 32-bit system bus
- Multi-instruction fetch in parallel with execution
- Automatic stack fills and spills in hardware
- Posted writes
- Hardware assist to single-and-double-precision IEEE floating-point instructions
- Fully static design
- JTAG support
- FPGA hardware simulation on custom SEP board

Software Development

The IGNITE cores are supported by the industry's leading development environments including optimized compilers:

- ANSI C
- GNU C/C++

Modeling tools are available to accelerate time to market through parallel software and hardware development:

- FPGA simulation board provides fast emulation Capability
- Cycle Accurate Model provides additional timing information for core operation

Deliverables

- Synthesizable RTL (Binary and source licenses available)
- Installation and configuration tools
- Synthesis, scan and ATGP script
- Gate-level simulation and verification
- Pre- and Post-Layout Timing Analysis script
- Software development tools: Compiler, Debugger, Assembler, Linker, Utilities
- Reference manual for processor core
- User's manual for development tools
- C program emulation of processor core
- IP emulation hardware platform
- Hard macro documentation

On-chip Debug Features

Each core's JTAG interface allows a debug host to set hardware breakpoints, examine or change memory and register values, and step through the target code.

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